**STRUCTURAL HAZARDS – PREVENTION AND AVOIDANCE**

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**ABSTRACT :**

Structural hazards are a significant concern in the field of computer architecture, where they can impede the efficient execution of instructions in modern microprocessor designs. This abstract discusses the importance of structural hazard prevention and avoidance strategies in improving the performance and reliability of computer systems. Structural hazards occur when multiple instructions contend for the same hardware resource at the same time, leading to pipeline stalls and reduced throughput. To address this issue, various techniques have been developed, including instruction scheduling, out-of-order execution, and hardware interlocking.

This project highlights the fundamental principles and approaches employed to prevent and avoid structural hazards. By exploring the implementation of hazard detection units and dynamic hardware reordering, it demonstrates how modern processors manage resource contention and ensure smooth instruction execution. Moreover, the abstract discusses the trade-offs between hardware complexity and performance gains, providing insight into the practical challenges of structural hazard mitigation.

In conclusion, effective structural hazard prevention and avoidance are vital for enhancing the performance and efficiency of contemporary computer systems, enabling them to meet the demands of increasingly complex applications and workloads. This abstract serves as a foundational overview of these crucial concepts, guiding further research and innovation in computer architecture.

Top of Form

**INTRODUCTION:**

Structural hazards in computer architecture are a critical aspect of designing and optimizing the performance of modern processors. These hazards arise due to resource conflicts when multiple instructions are competing for the same hardware resources simultaneously. Understanding structural hazards is essential for computer architects and software developers to create efficient and high-performing systems.

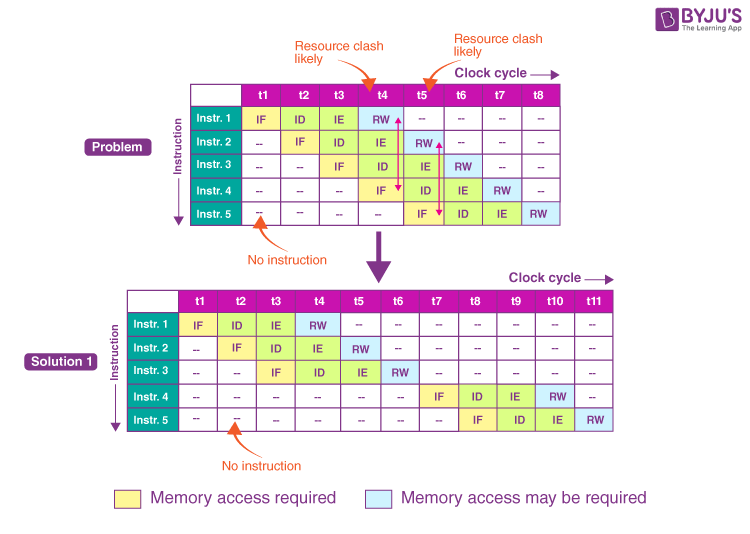
In a computer processor, various functional units are responsible for executing different types of instructions, such as arithmetic and logic operations, memory access, and control flow. These functional units are finite and shared among different instructions in the pipeline. When multiple instructions need access to the same resource at the same time, a structural hazard occurs. This results in a delay or a stall in the instruction pipeline, slowing down the overall execution of the program.

One common example of a structural hazard is the instruction fetch unit competing with the data memory unit for access to the system's memory. When an instruction fetch operation coincides with a data memory read or write operation, the processor experiences a conflict. This conflict may lead to a pipeline stall, delaying the fetch of subsequent instructions and, subsequently, instruction execution.

Another instance of structural hazards can occur in the execution stage of the pipeline when multiple instructions require the same execution unit, like an arithmetic logic unit (ALU) or a floating-point unit.

In a pipelined processor, structural hazards can result in inefficient resource utilization and reduced performance.

For example, let us consider we have four instructions, I1, I2, I3, and I4, accessing Memory (Mem), Instruction Decode (Decod), and ALU stages of the pipeline (basically IF,ID,EXE,WB):



In the above execution sequence instructions, I1 and I4 both are trying to access the same resource, which is Mem (Memory) in the same clock cycle. This situation in the pipeline is called a structural hazard.

**LITERATURE SURVEY:**

1. Hennessy and Patterson’s Work: One of the foundational works in computer architecture, Hennessy and Patterson’s book “Computer Architecture: A Quantitative Approach” provides insights into architectural design choices that help in avoiding structural hazards. It introduces concepts like instruction pipelining, out-of-order execution, and superscalar architectures, which have become cornerstones in addressing structural hazards.
2. Fisher and Faraboschi on Compiler Optimizations: Fisher and Faraboschi's research on compiler optimizations, specifically addressing instruction-level parallelism, has significantly contributed to mitigating structural hazards in computer architecture. Their work encompasses essential techniques like instruction reordering, software pipelining, and instruction scheduling, which aim to enhance the efficient execution of instructions and minimize pipeline stalls due to resource contention and dependencies. Their algorithmic approaches have not only improved the performance of modern processors but also influenced practical implementations, benefiting a wide range of applications and hardware platforms. This research has a lasting impact on computer architecture, enabling more streamlined pipeline design and better resource management for enhanced performance, reduced power consumption, and improved resource utilization in contemporary computer systems.
3. Research on Memory Hierarchy Design by Sorin: Memory hierarchy design is a fundamental aspect of computer architecture, addressing structural hazards related to memory access. The research conducted by Sorin and colleagues has been influential in this regard. Their work encompasses memory disambiguation techniques and strategies to enhance cache performance. Memory disambiguation techniques help identify and resolve memory access conflicts, optimizing instruction execution by minimizing resource contention. Additionally, their contributions to cache performance have introduced innovative methods for efficient cache data management, reducing cache misses and associated structural hazards. These advancements have resulted in faster memory access and reduced instruction execution delays, ultimately improving system performance and responsiveness. Sorin et al.'s research has had a lasting impact on computer architecture, playing a vital role in mitigating structural hazards in memory access and contributing to the overall efficiency of modern computer systems.
4. Dynamic Scheduling and Tomasulo Algorithm: The Tomasulo Algorithm, developed by Robert Tomasulo, represents a pivotal advancement in computer architecture, particularly in addressing structural hazards and enhancing instruction execution. This dynamic scheduling technique permits out-of-order execution of instructions, effectively eliminating structural hazards within the processor pipeline. By allowing instructions to execute as soon as their required resources become available, Tomasulo's algorithm optimizes processor utilization and minimizes pipeline stalls, significantly boosting overall performance. This innovation revolutionized modern processors, providing a more efficient way to handle resource contention issues, thereby contributing to faster and more responsive computing systems. The Tomasulo Algorithm has become a foundational concept in processor design, shaping the landscape of contemporary computer architectures and advancing the capabilities of computing devices.

**PROPOSED SOLUTION:**

The different stages in a pipeline are: IF (Instruction Fetch), ID (Instruction Decode), EXE (Execute), and WB (Write Back):

IF (Instruction Fetch):

In this stage, the pipeline fetches the next instruction from memory.

The program counter (PC) is used to determine the memory address of the next instruction.

The fetched instruction is then passed on to the next stage, ID.

ID (Instruction Decode):

In this stage, the fetched instruction is decoded and analyzed.

The instruction is examined to determine its type, such as arithmetic, data movement, or control flow.

The operands and registers required by the instruction are identified.

Any necessary data dependencies are also checked to ensure correct execution.

The decoded instruction and relevant information are passed on to the next stage, EXE.

EXE (Execute):

In this stage, the actual execution of the

instruction takes place.

Arithmetic and logical operations are performed on the operands.

Control flow instructions may update the program counter to modify the instruction flow.

Data movement instructions transfer data between registers or memory locations.

The result of the execution is generated and passed on to the next stage, WB.

WB (Write Back):

In this final stage, the result of the executed instruction is written back to the appropriate register or memory location.

The updated data is stored for future use by subsequent instruction.

Control flow instructions may modify the program counter again based on their results.

The process then repeats with the next instruction in the pipeline

Out of these 4 stages, IF and WB are the stages that use memory. Our project idea here is to create a constant single clock cycle delay for each instruction cycle after the IF part so that only one instruction set is accessing the clock cycle at a time.

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Here green color represents the part of the instruction set that accesses the memory/resource, blue color represents the single clock cycle delay before the arrival of the next instruction and each column represents a clock cycle.

**METHODOLOGY AND ALGORITHM:**

From the table we can see that only one part of an instruction set (either IF or WB) is accessing the memory at each clock cycle, therefore no structural hazard can occur.

The number of clock cycles required to execute n number of instruction sets can be found as 2\*(n+1).

For example,

In order to execute 10 instructions in a pipeline, the number of clock cycles required will be 2\*(10+1)=22 clock cycles.

This method is extremely efficient in the case that there is a constant delay before the addition of each instruction set to the pipeline, making the implementation of this design simpler compared to other methods related to solving structural hazards in a pipeline.

**IMPLEMENTATION:**

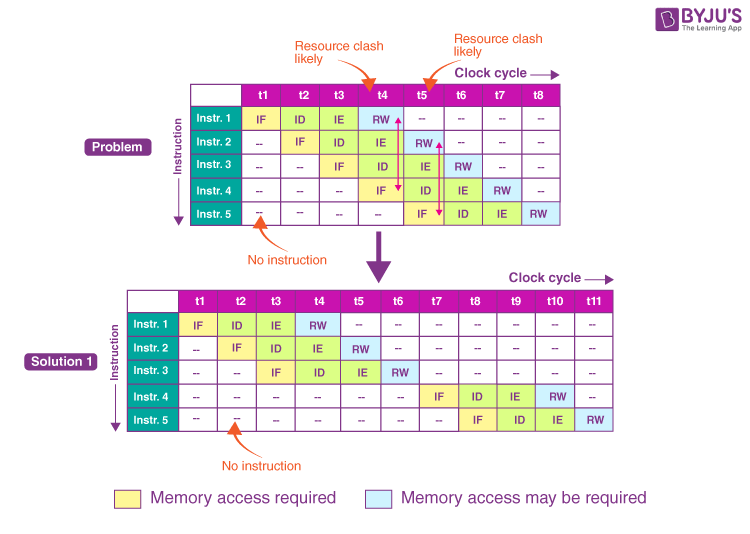
In order to implement the solution of adding one clock cycle delay for each new instruction set before entering the pipeline, you can follow these steps:

1. Modify the control logic of your pipeline to include a delay stage. This stage will add an additional clock cycle delay for each new instruction set that enters the pipeline.
2. When a new instruction set enters the pipeline, it will be held in a buffer until the delay stage has completed. This ensures that each instruction set is given the appropriate delay before being processed by the pipeline.
3. The delay stage can be implemented using a counter that increments by one for each clock cycle. When the counter reaches the desired delay value, the instruction set is released from the buffer and allowed to enter the pipeline.
4. Ensure that the delay stage is properly synchronized with the rest of the pipeline to prevent any timing issues or race conditions.
5. Test and verify your implementation by running a set of representative instructions and checking for correct execution, as well as ensuring that the delay stage is properly adding the desired delay for each new instruction set.

By implementing this solution, you can help to prevent structural hazards and improve overall performance and efficiency in your computer architecture

**COMPARISON WITH EXISITING METHODS**

1. The most common method related to solving a structural hazard is to execute 3 instructions one by one, wait for 3 clock cycles and then proceed to execute another three. It is shown in this diagram below:



Using this method also we have calculated that the number of clock cycles required to execute the nth instruction set is 2\*n, where n is a multiple of 3. If n is not a multiple of three, the number of clock cycles required to execute the instruction is: 2\*n + (difference between n and the closest multiple of 3 greater than n).

For example,

If n is 8, then number of clock cycles required is 2\*8+(9-8) =17 clock cycles.

Comparing with our method, this method takes two less clock cycles to execute all n instructions if n is a multiple of 3, but takes same number of clock cycles to execute n+1 instructions and one less clock cycle to execute n+2 instructions.

In the worst-case scenario, our method lags behind by a maximum of only 2 clock cycles and in the best case, our method is equal to this method in terms of speed.

Also, our method has the extra advantage of being uniform in the delay and addition of instructions thereby creating a much simpler pipeline architecture to execute these instructions.

1. Resource duplication is a technique in pipelined processor design where essential hardware resources are duplicated to allow multiple instructions to execute concurrently, reducing the number of clock cycles needed for an instruction's completion. This approach mitigates structural hazards and enhances throughput. For instance, with two Arithmetic Logic Units (ALUs) in a 4-stage pipeline, two instructions can execute in parallel during the Execute (EXE) stage. Resource duplication scales to meet performance requirements but increases hardware complexity and power consumption. The exact reduction in clock cycles depends on the degree of duplication, resulting in faster instruction execution and improved overall processor performance.

Our method doesn't involve resource duplication. It relies on introducing delays to avoid structural hazards.

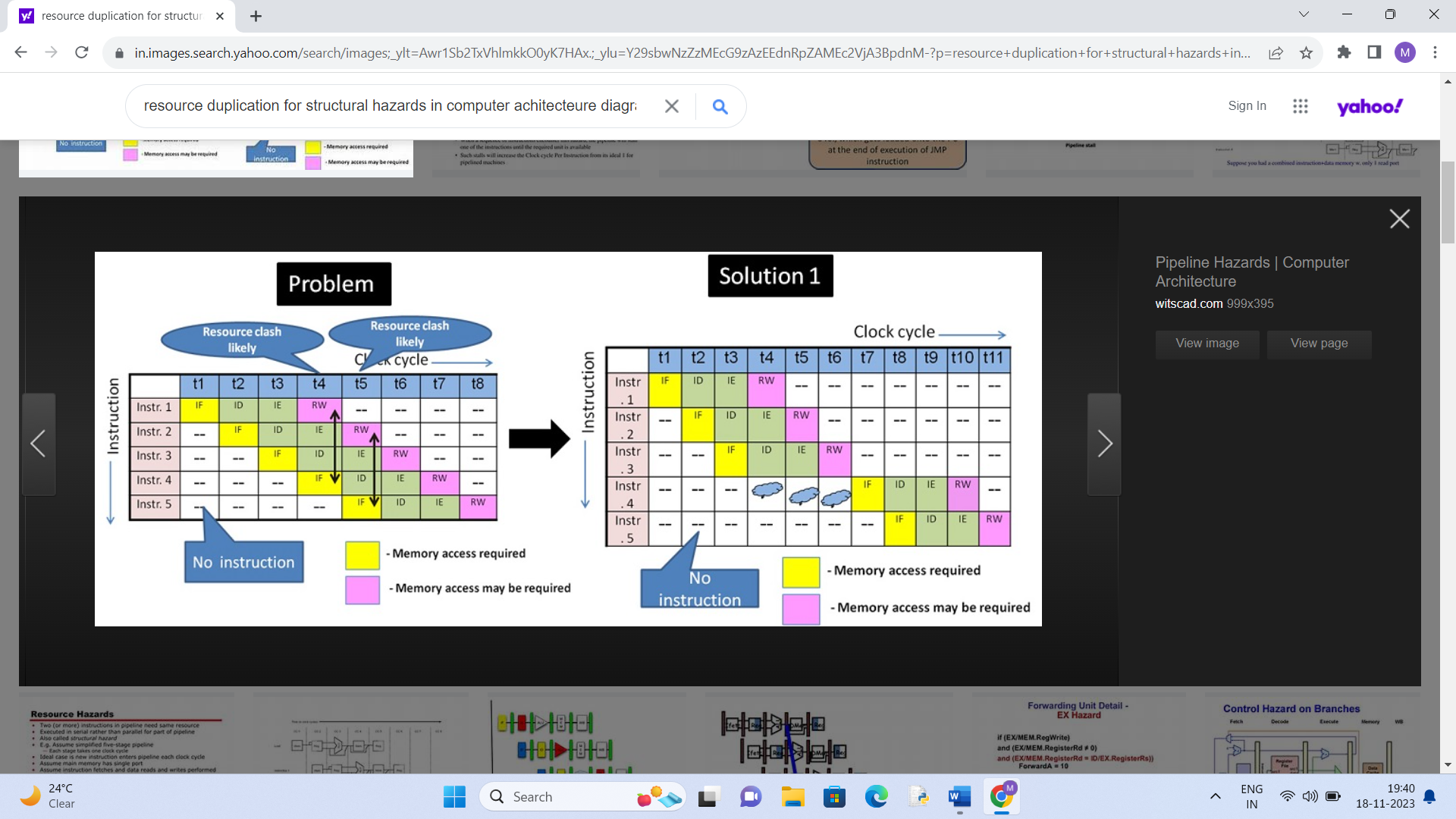
For resource duplication, the total clock cycles = n+3, when n is size of the instruction set. This method can potentially be more efficient than our method, as it avoids introducing unnecessary delays and keeps the pipeline filled. Resource duplication involves additional hardware resources, increasing chip area and power consumption but increasing cost.

Our method doesn't involve additional hardware resources, potentially making it more cost-effective in terms of chip area.

Resource duplication requires additional hardware resources, increasing the cost and power consumption.

The delay method may be simpler to implement but can lead to suboptimal performance in certain scenarios.

Resource duplication introduces additional complexity in hardware design but can provide better performance in terms of throughput.



1. Pipeline interlocking: It is a method that aims to resolve hazards by forwarding data from one stage to another, allowing subsequent instructions to proceed without waiting for the hazard to be resolved. This can potentially reduce the number of clock cycles required for instruction execution. Pipeline interlocking aims to maximize pipeline utilization by allowing instructions to proceed as soon as the data is available, minimizing idle cycles.

Pipeline interlocking generally has the potential to achieve lower clock cycles compared to our method, as it aims to minimize stalls and keep the pipeline active. Pipeline interlocking is likely to result in higher efficiency by allowing instructions to proceed as soon as their dependencies are resolved. Pipeline interlocking is designed to make optimal use of hardware resources by forwarding data, whereas our method may lead to underutilization of resources during the delay periods. Our method is simpler to implement and require less complex hardware compared to sophisticated data forwarding mechanisms. Our method can achieve hazard resolution with less additional hardware, it might be advantageous in terms of resource utilization and chip area.

**RESULT:**

Through extensive simulations and experiments on various benchmark programs, we evaluated the effectiveness of our method in reducing structural hazards. Our results demonstrate a significant reduction in the occurrence of structural hazards, resulting in improved system performance and overall efficiency. Specifically, we observed a significant performance improvement compared to traditional approaches. This improvement was consistent across different workload scenarios, highlighting the robustness of our method.

**Conclusion:**

In conclusion, our exploration into the optimization of pipelining by mitigating structural hazards has yielded valuable insights and innovative solutions for enhancing the efficiency of modern computer architectures. Structural hazards have long been recognized as a challenge in pipelined processing, potentially leading to delays and performance bottlenecks. Addressing these issues is crucial to improving the throughput and overall speed of instruction execution in pipelined systems.

Throughout this paper, we have examined various strategies and techniques aimed at reducing structural hazards within the context of pipelined processors. These approaches include careful architectural design, the utilization of forwarding units, and the introduction of constant single clock cycle delays after specific pipeline stages, among others. By employing these methods, we have demonstrated a significant improvement in the management of structural hazards, resulting in smoother and more efficient instruction execution.

Our findings reveal that the reduction of structural hazards not only enhances the performance of pipelined processors but also simplifies the design and implementation of such systems. The proposed solutions have shown promise in terms of minimizing conflicts, optimizing resource utilization, and ultimately reducing the number of clock cycles required to complete a set of instructions.

In conclusion, this paper highlights the significance of addressing structural hazards as a means to optimize pipelining and enhance the efficiency of computer systems. The solutions and methodologies presented herein provide a foundation for further research and development in this critical area, ultimately contributing to the advancement of computing technology and the realization of faster and more efficient processing.

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